Xilinx VSK BareBone

I have a Xilinx Spartan3A-based Video Starter Kit (comes complete with camera daughterboard and DVI output). However, I do not want to use the Microblaze-based system created using EDK. I want to create a full custom design from scratch using ISE.

Software Preparation

Using ISE 12.1 (Vivado does not support Spartan devices and ISE 14 is absurdly big) on Slackware 14.1.

Installation

Needs to be done as root (even when target path is writable by normal user).

Running

Needs QT_PLUGIN_PATH variable to be null (or maybe just set ISE path before existing??). I set everything in my start-up script discussed here. The latest version is always available at my GitHub site.

Cable Setup

Requires fxload and cable usb driver (Git here). Installation steps are given in the README file.

Board Information

Pin Information

- FPGA Clocking
  - Clock generator: IDT5V9885PFGL
  - Output: 4_N, FPGA Pin: AE13, Default Frequency: 31.25MHz
  - Output: 6, FPGA Pin: AF13, Default Frequency: 27MHz
  - **[20150410] VERIFIED! DETAILS LATER…**
- RS232 Serial Port (need a pin to probe signal!)
  - FPGA Pin: V14, TX
  - FPGA Pin: AA20, RX

- LEDs:
  - FPGA Pin: W23, LED DS10
  - FPGA Pin: V22, LED DS11
  - FPGA Pin: V25, LED DS12
  - FPGA Pin: V24, LED DS13
- Switches:
  - FPGA Pin: N25, # S4 NORTH
  - FPGA Pin: N26, # S5 WEST
  - FPGA Pin: Y26, # S6 CENTER
  - FPGA Pin: N23, # S7 EAST
  - FPGA Pin: P21, # S8 SOUTH
- Soft-touch connectors:
  - FPGA Pin: H2, Soft-touch A1 (FMC_LA03_P)
  - FPGA Pin: H1, Soft-touch A2 (FMC_LA03_N)
  - FPGA Pin: J5, Soft-touch A4 (FMC_LA14_P)
  - FPGA Pin: J4, Soft-touch A5 (FMC_LA14_N)
- FMC#1 Connectors:
  - FPGA Pin: L4, FMC#1 C10 (0_LA06_P)
  - FPGA Pin: L3, FMC#1 C11 (0_LA06_N)
  - FPGA Pin: M2, FMC#1 D01 (PGC2M)
  - FPGA Pin: D3, FMC#1 D11 (0_LA05_P)
  - FPGA Pin: E4, FMC#1 D12 (0_LA05_N)
- Misc.:
  - FPGA Pin: R9, # set: 1 to use FMC#1, 0 to use memory

to be continued...

Project from Scratch

Some notes on the things I try to build from 'scratch'.

Check Clock Signal

I start with something simple:

- define 2 input clock pins
- use clock signal to generate basic square-waveform
- also try to control basic input (switch) and output (led)

my1fpga.vhdl

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to be continued...

From:
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